Terms used
EEPROM EPROM flash address polling most significant bit

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1 The CAN microcluster: Parallel processing over the controller area network

Paul A. Kuban, Rammohan K. Ragade

March 2005 **Journal on Educational Resources in Computing (JERIC)**, Volume 5 Issue 1

Publisher: ACM Press

Full text available: pdf(242.37 KB) Additional Information: full citation, abstract, references, index terms

Most electrical engineering and computer science undergraduate programs include at least one course on microcontrollers and assembly language programming. Some departments offer legacy courses in C programming, but few include C programming from an embedded systems perspective, where it is still regularly used. Distributed computing and parallel processing are subjects generally reserved for graduate programs or specialized degrees. And although it is common to provide undergraduate courses on c ...

Keywords: CAN, Cluster, controller area network, distributed, embedded systems, microcontrollers, parallel

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#11	((((EEPROM or EPROM OR PROM or ROM or FLASH <IN>metadata)) <AND> (((top or bottom) and decod*<IN>metadata))) <AND> (nonvolatile memory)) <AND> (((most significant bit) or MSB<IN>metadata))
#12	(((((EEPROM or EPROM OR PROM or ROM or FLASH <IN>metadata)) <AND> (((top or bottom) and decod*<IN>metadata))) <AND> (nonvolatile memory)) <AND> (((most significant bit) or MSB<IN>metadata))) <AND> ((pin<IN>metadata))

[redacted]

Indexed by Inspec

A 90-nm CMOS 1.8-V 2-Gb NAND flash memory for mass storage applicatior

Lee, J. Sung-Soo Lee Oh-Suk Kwon Kyeong-Han Lee Dae-Seok Byeon In-Young Kim Kyoung-Hwa Lee Youn Soon Choi Jong-Sik Lee Wang-Chul Shin Jeong-Hyuk Choi Kang-Deog Suh
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This paper appears in: Solid-State Circuits, IEEE Journal of
Publication Date: Nov. 2003
Volume: 38 , Issue: 11
On page(s): 1934 - 1942
ISSN: 0018-9200
INSPEC Accession Number:7778183
Digital Object Identifier: 10.1109/JSSC.2003.818143
Posted online: 2003-10-27 09:52:48.0

Abstract
A 1.8-V 2-Gb NAND flash memory has been successfully developed on a 90-nm CMOS STI process technology, resul 2/ die size and a 0.044-/spl mu/m/sup 2/ effective cell. For the higher level integration, critical layers are patterned with The device has three notable differences from previous generations. 1) The cells are organized in a single (16K+512) c array by adopting a one-sided row decoder in order to minimize the die size. 2) The bitline precharge level is set to 0.9 on-cell current. 3) During the program operations, the string select line, which connects the NAND cell strings to the bitl sub-V/sub CC/ in order to avoid program disturbance issues.

Index Terms
Inspec
Controlled Indexing
CMOS memory circuits NAND circuits flash memories integrated circuit layout memory architecture photolithography

Non-controlled Indexing
1.8 V 2 Gbit 90 nm CMOS NAND flash memory CMOS STI process technology KrF photolithography strings bitline precharge level block placement chip architecture critical layer patterning die size minimi effective cell higher level integration mass storage applications on-cell current one-sided row decoder disturbance avoidance string select line

Author Keywords
Not Available

References

1 T. H. Cho, et al., "A dual-mode NAND flash memory: 1-Gb multilevel and high-performance 512-Mb single-level m *State Circuits*, vol. 36, pp. 1700-1706, Nov. 2001.
Abstract | Full Text: PDF (295KB)

2 K. Imamiya, et al., "A 125-$\\hbox{mm}^{2} $ 1-Gb NAND flash memory with 10-Mbyte/s program speed," *IEEE J.* vol. 37, pp. 1493-1501, Nov. 2002.
Abstract | Full Text: PDF (849KB)

3 J. Lee, et al., "High-Performance 1-Gb NAND flash memory with 0.12-$\\mu \\hbox{m}$ technology," *IEEE J. Solid* 37, pp. 1502-1509, Nov. 2002.
Abstract | Full Text: PDF (696KB)

4 T. Tanaka, et al., "A quick intelligent page-programming architecture and a shielded bitline sensing method for 3 V memory," *IEEE J. Solid-State Circuits*, vol. 29, pp. 1366-1373, Nov. 1994.
Abstract | Full Text: PDF (612KB)

5 K. D. Suh, et al., "A 3.3 V 32 Mb NAND flash memory with incremental step pulse programming scheme," *IEEE J.* vol. 30, pp. 1149-1156, Nov. 1995.
Abstract | Full Text: PDF (1028KB)

6 K. Takeuchi, et al., "A source-line programming scheme for low-voltage operation NAND flash memories," *IEEE J.* vol. 35, pp. 672-681, May 2000.
Abstract | Full Text: PDF (516KB)

7 S. Satoh, et al., "A novel channel boost capacitance (CBC) cell technology with low program disturbance suitable f 4 Gbit NAND flash memories," *Symp. VLSI Technol. Dig. Tech. Papers*, pp. 108-109, June 1998.
Abstract | Full Text: PDF (212KB)

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L2	8	(Antonino near2 Malfa).in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/21 13:51
L3	12	(Salvatore near2 Poli).in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/21 13:51
L4	12	(Paolino near2 Schillaci).in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/21 13:51
L5	12	(Paolino near2 Schillaci).in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/21 13:51
L6	12	(Salvatore near2 Poli).in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/21 13:51
L7	8	(Antonino near2 Malfa).in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/21 13:51
L8	6	L5 and L6 and L7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/21 13:51
L9	48036	nonvolatile adj memory	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/21 13:51

EAST Search History

L10	105924	flash adj memory	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/21 13:51
L11	440041	eeprom or eprom or rom	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/21 13:51
L12	35034	select$4 adj memory	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/21 13:51
L13	121677	select$4 near3 memory	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/21 13:51
L14	17311	decod$4 same (top or bottom)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/21 13:51
L15	121677	select$4 near3 memory	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/21 13:51
L16	17311	decod$4 same (top or bottom)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/21 13:51
L17	2928	L15 and L16	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/21 13:51
L18	275	L15 same L16	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/21 13:51
L19	1482538	pin$2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/21 13:51

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L20	275	L15 same L16	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/21 13:51
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L22	55	L20 and L21	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/21 13:51
L23	5	L20 same L21	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/21 13:52
L24	41331	(most adj significant adj bit) or MSB	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/21 13:53
L25	248	(memory adj address) same poll$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/21 13:54
L26	41	24 and 25	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/21 13:54
L27	0	23 and 26	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/21 13:54
L28	30010	"711"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/21 13:54
L29	73086	"365"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/21 13:55

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L30	5	26 and 28	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/21 13:55
L31	3	26 and 29	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/21 13:56
L32	4	1 and 30	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/21 13:56
L33	3	1 and 31	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/21 13:56
L34	0	23 and 32	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/21 13:56
L35	0	23 and 33	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/07/21 13:56